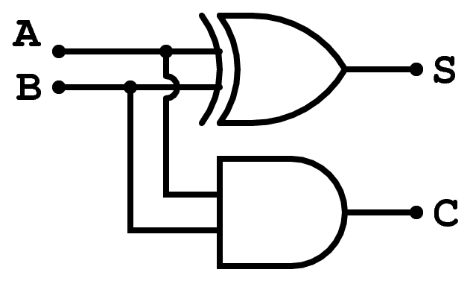
**EXPERIMENT NO.1**

AIM: To design the circuit of half adder.

IC USED: 7486(X-OR), 7408(AND).

THEORY: A half adder is a logical circuit that performs an additional operation on two binary digits. The half adder produces a sum and a carry value which are both binary digits.

A half adder circuit has two inputs A and B and two outputs – S representing sum and C representing carry.



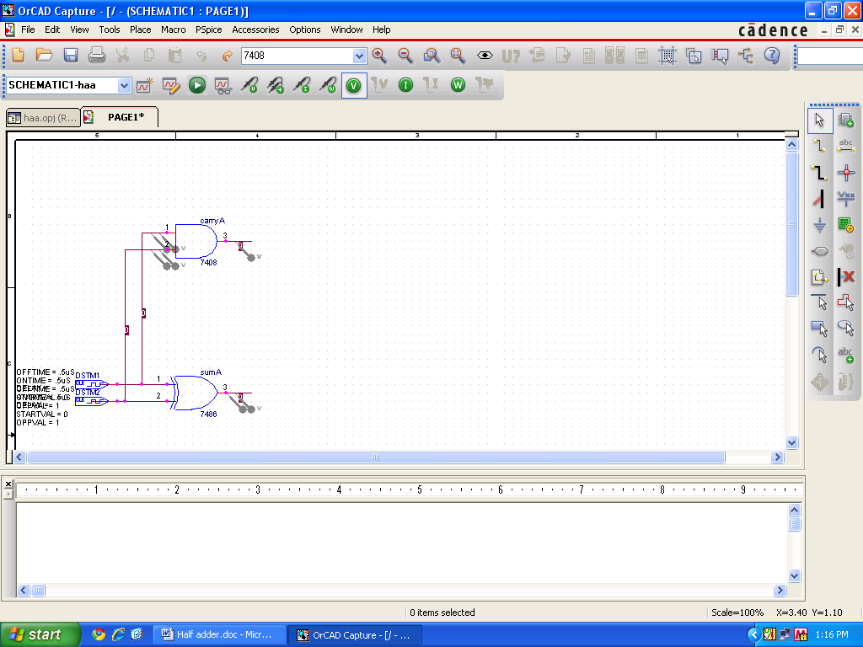
S = A xor B i.e. (A’B + AB’)

C = A and B i.e. (A.B)

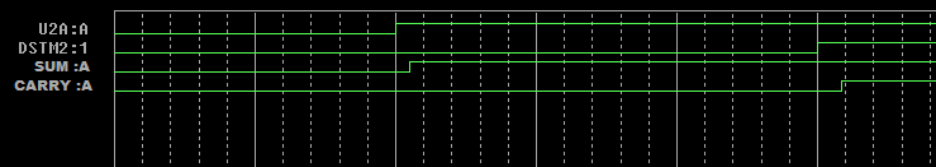
TRUTH TABLE:

| **A** | **B** | **S** | **C** |
| --- | --- | --- | --- |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

SCHEMATIC DIAGRAM:



WAVEFORM:



RESULT: The output waveform of half adder is verified.